

第12章

DSP Builder设计深入

12.1 FIR数字滤波器设计

12.1.1 FIR滤波器原理

$$H(z) = \sum_{k=0}^M b_k z^{-k} \quad (12-1)$$

$$y(n) = \sum_{i=0}^{L-1} x(n-i)h(i) \quad (12-2)$$

$$y(n) = x(n)h(n) \quad (12-3)$$

12.1 FIR数字滤波器设计

12.1.1 FIR滤波器原理

$$y(n) = h(0)x(n) + h(1)x(n-1) + h(2)x(n-2) + h(3)x(n-3) \quad (12-4)$$

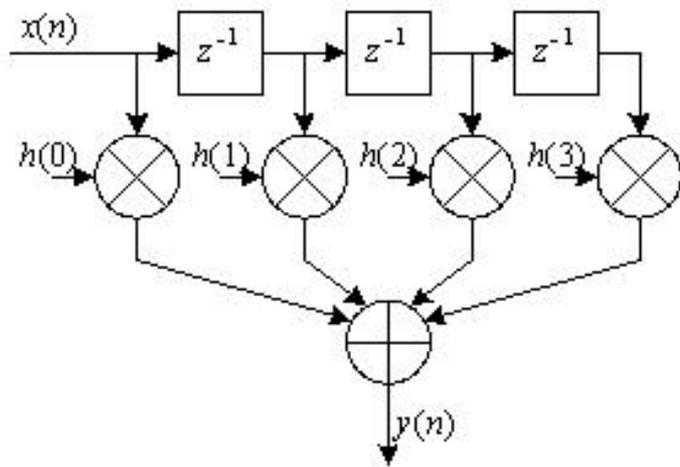


图 12-1 3阶 FIR 滤波器结构

12.1 FIR数字滤波器设计

12.1.2 使用DSP Builder设计FIR滤波器

1. 3阶常数系数FIR滤波器设计

$$h(n) = C_q (h(0)x(n) + h(1)x(n-1) + h(2)x(n-2) + h(3)x(n-3)) \quad (12-5)$$

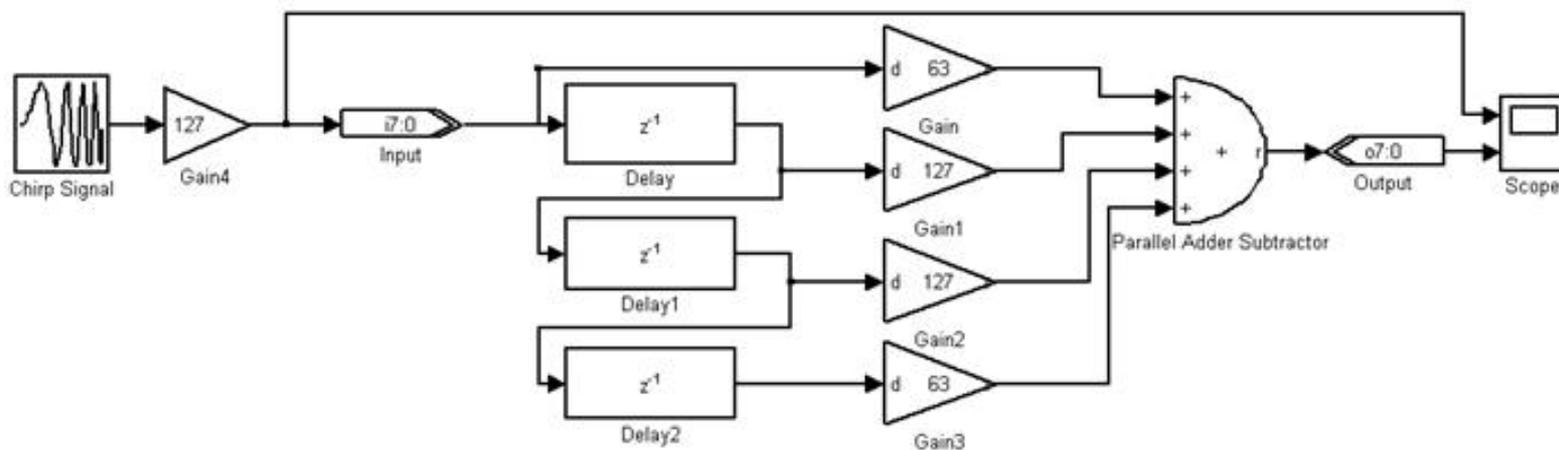


图 12-2 带有仿真信号模块的 3 阶滤波器模型

12.1 FIR数字滤波器设计

12.1.2 使用DSP Builder设计FIR滤波器

1. 3阶常数系数FIR滤波器设计

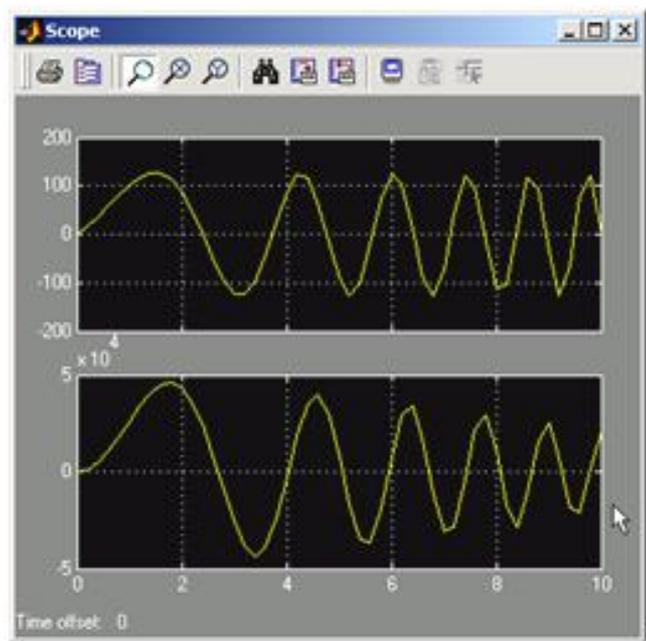


图 12-3 FIR 滤波器仿真结果

12.1 FIR数字滤波器设计

12.1.2 使用DSP Builder设计FIR滤波器

2. 4阶FIR滤波器节设计

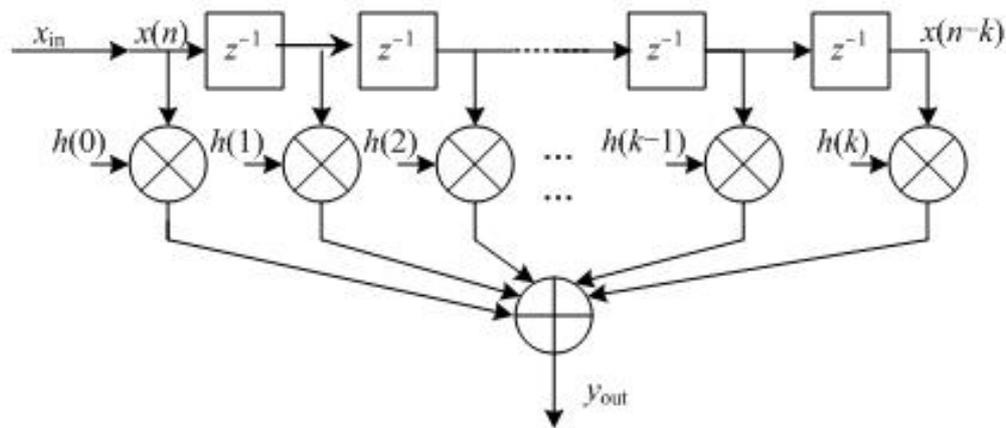


图 12-4 直接 I 型 FIR 滤波器结构

12.1 FIR数字滤波器设计

12.1.2 使用DSP Builder设计FIR滤波器

2. 4阶FIR滤波器节设计

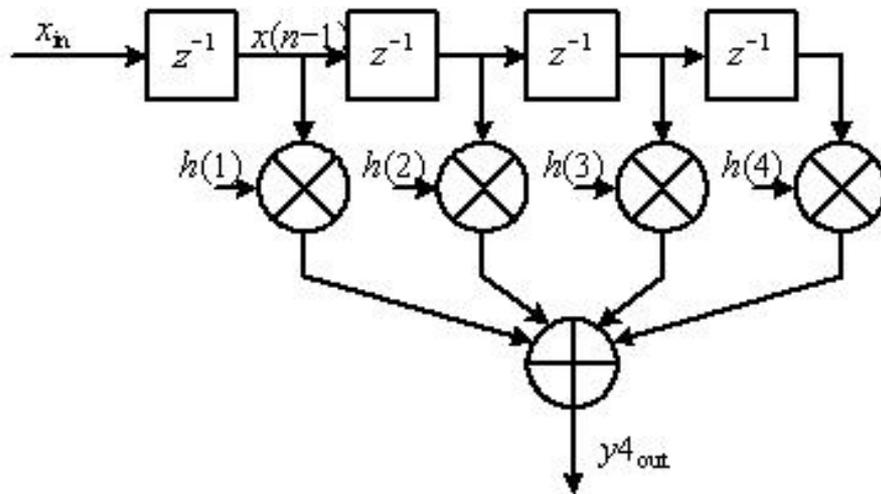


图 12-5 直接 I 型 4 阶 FIR 滤波器节

$$H(z) = h(1)z^{-1} + h(2)z^{-2} + h(3)z^{-3} + h(4)z^{-4}$$

(12-6)

12.1 FIR数字滤波器设计

12.1.2 使用DSP Builder设计FIR滤波器

2. 4阶FIR滤波器节设计

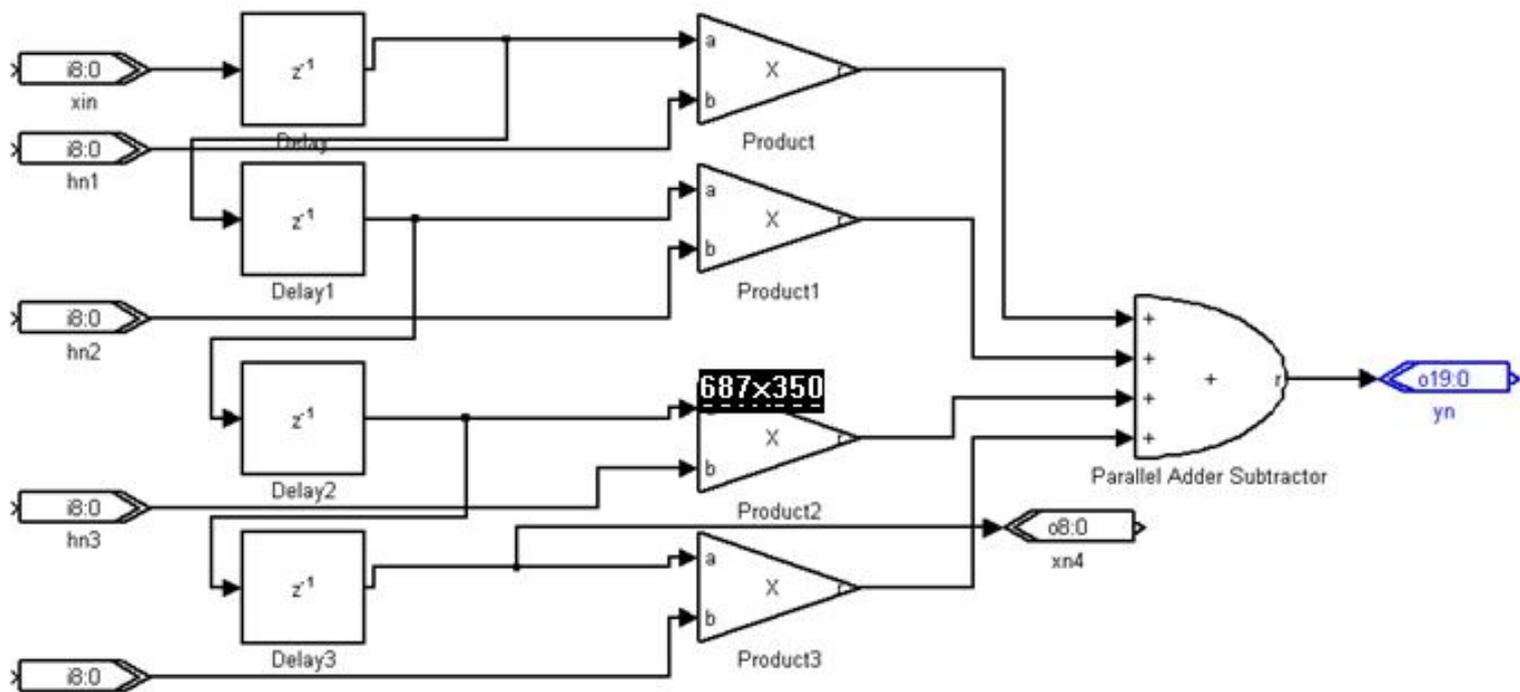


图 12-6 直接 I 型 4 阶 FIR 滤波器节

12.1 FIR数字滤波器设计

12.1.2 使用DSP Builder设计FIR滤波器

3. 16阶FIR滤波器模型设计

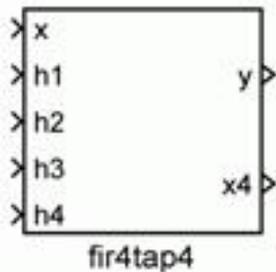


图 12-7 fir4tap 子系统

12.1 FIR数字滤波器设计

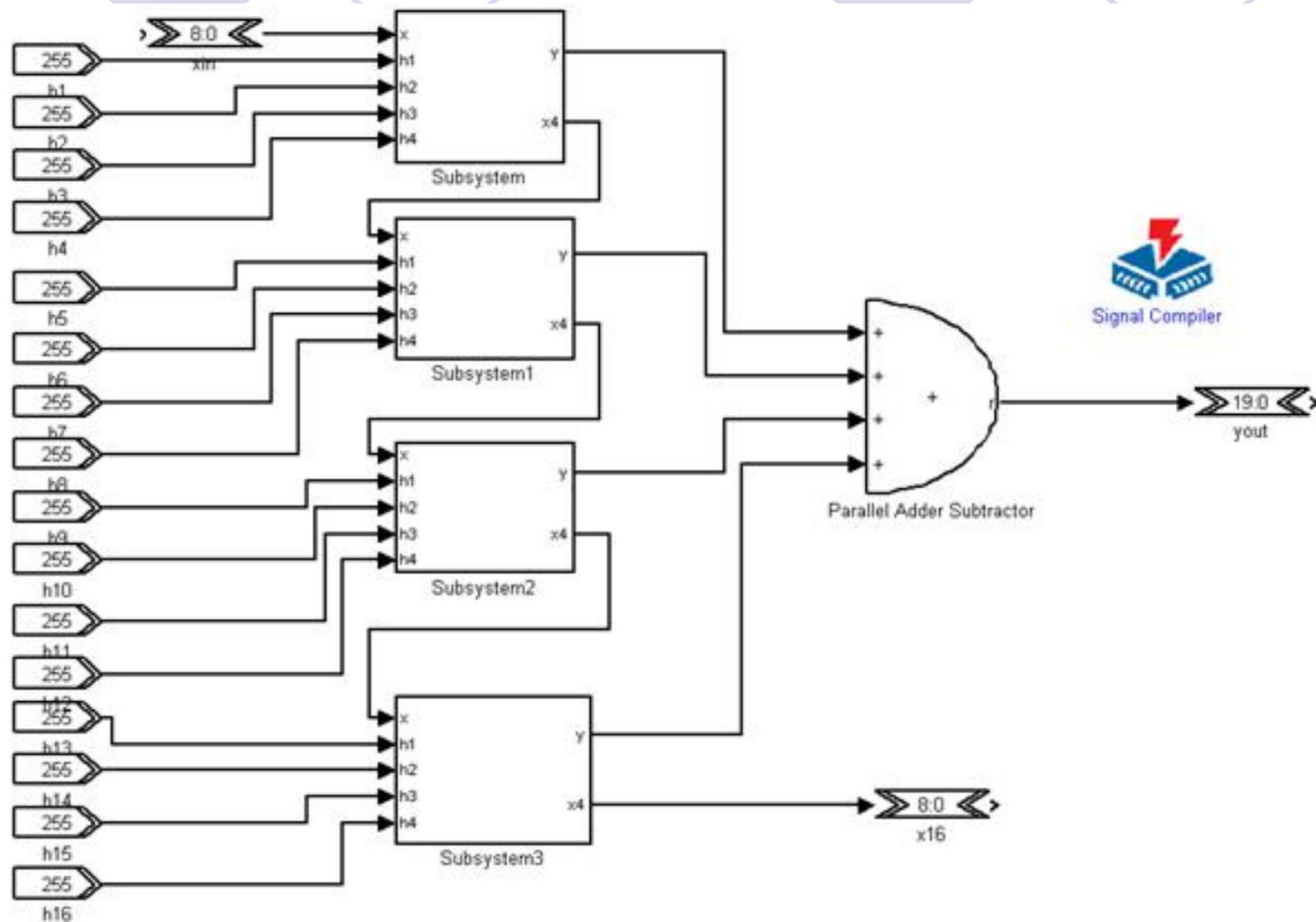


图 12-8 16 阶直接 I 型 FIR 滤波器模型

12.1 FIR数字滤波器设计

12.1.3 使用MATLAB的滤波器设计工具

1. 打开MATLAB的FDATool

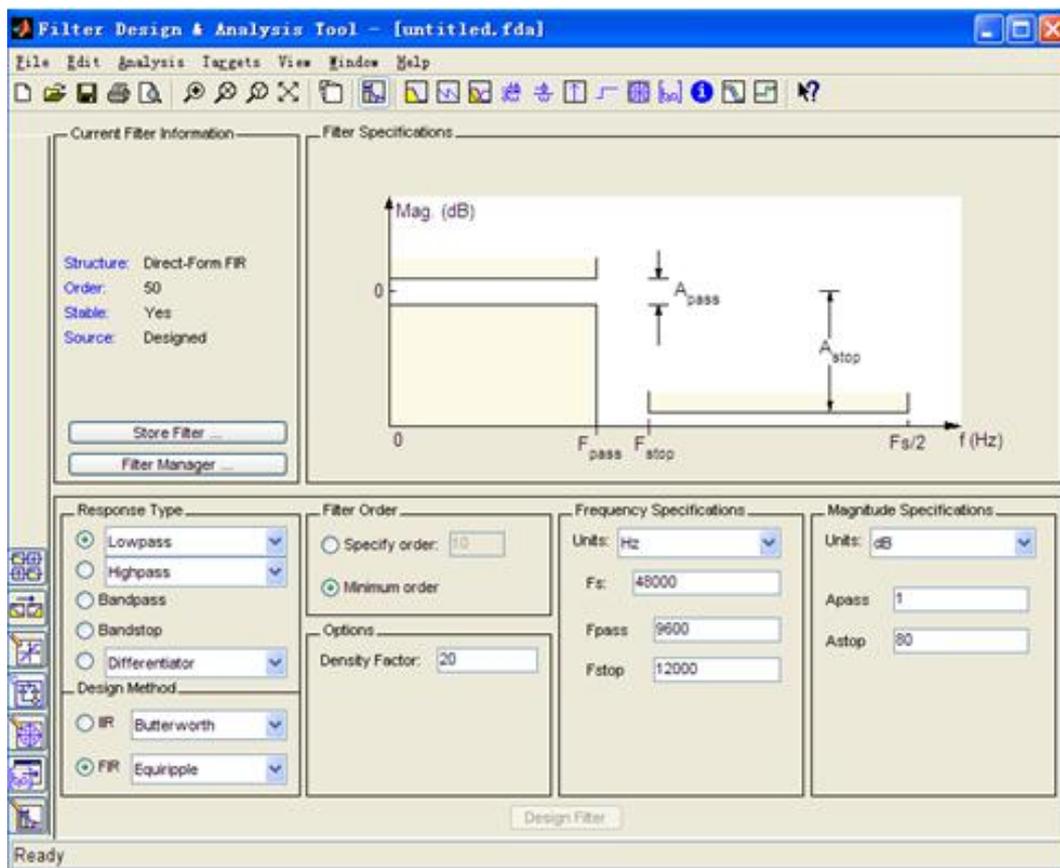


图 12-9 FDATool 界面

12.1 FIR数字滤波器设计

12.1.3 使用MATLAB的滤波器设计工具

2. 选择Design Filter

$$H(z) = \sum_{k=1}^{16} b_k z^{-k} \quad (12-7)$$

$$H(z) = z^{-1} \sum_{k=0}^{15} b_k z^{-k} \quad (12-8)$$

12.1 FIR数字滤波器设计

12.1.3 使用MATLAB的滤波器设计工具

3. 滤波器分析

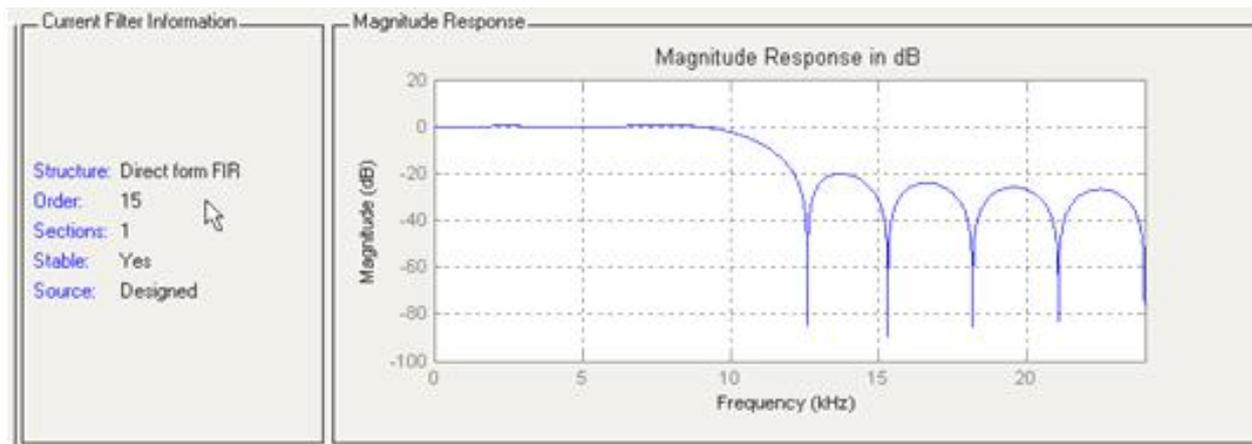


图 12-10 FIR 滤波器的幅频响应

12.1 FIR数字滤波器设计

12.1.3 使用MATLAB的滤波器设计工具

3. 滤波器分析

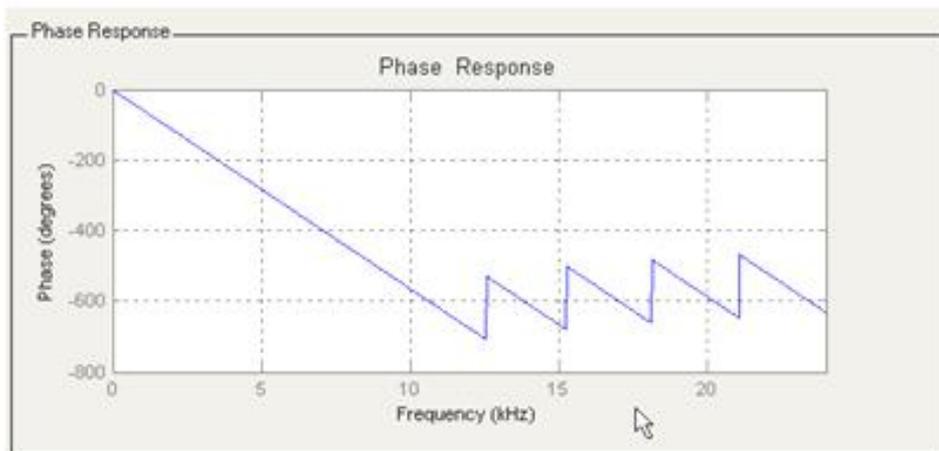


图 12-11 FIR 滤波器的相频响应

12.1 FIR数字滤波器设计

12.1.3 使用MATLAB的滤波器设计工具

3. 滤波器分析

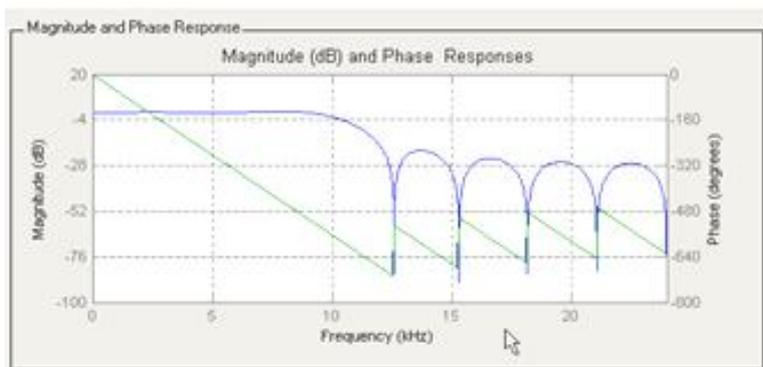


图 12-12 幅频响应与相频响应比较

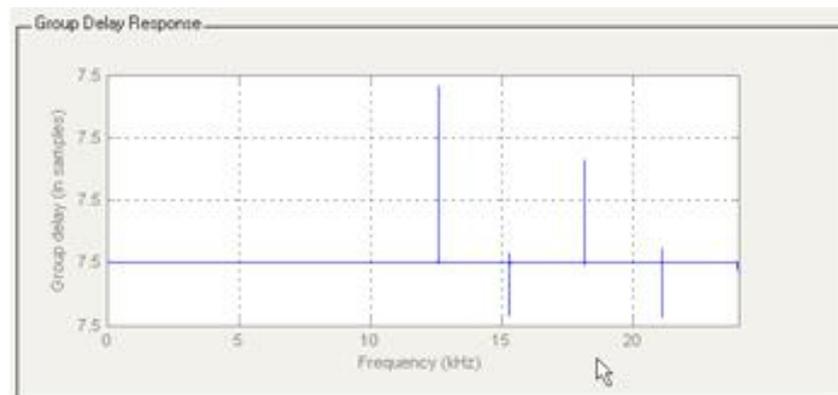


图 12-13 FIR 滤波器的群延时

12.1 FIR数字滤波器设计

12.1.3 使用MATLAB的滤波器设计工具

3. 滤波器分析

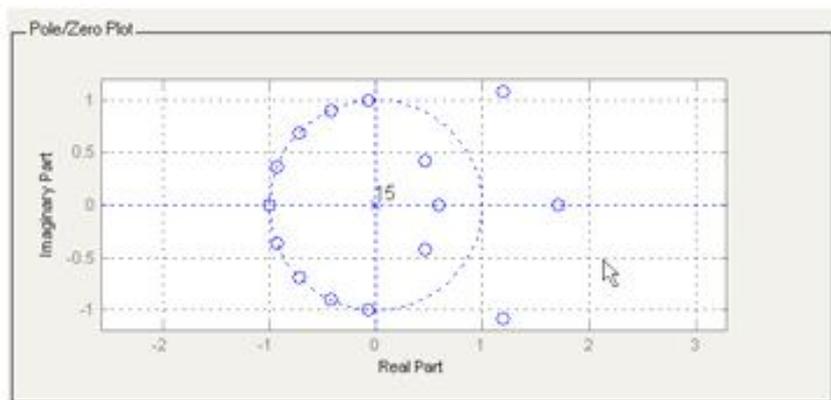


图 12-14 FIR 滤波器的零极点

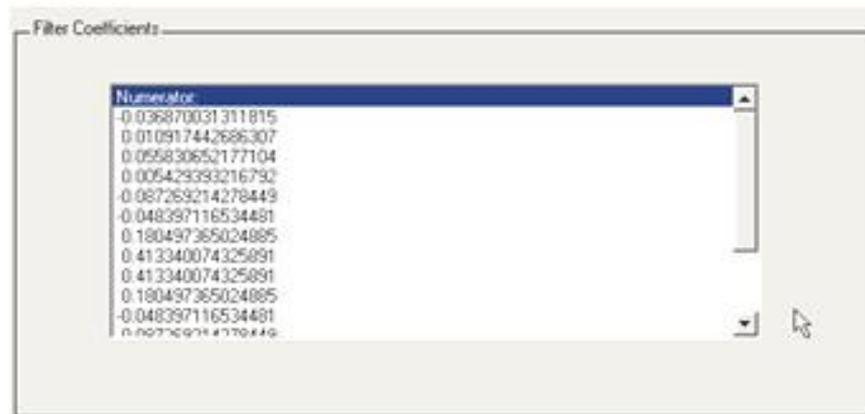


图 12-15 FIR 滤波器系数

12.1 FIR数字滤波器设计

12.1.3 使用MATLAB的滤波器设计工具

4. 量化

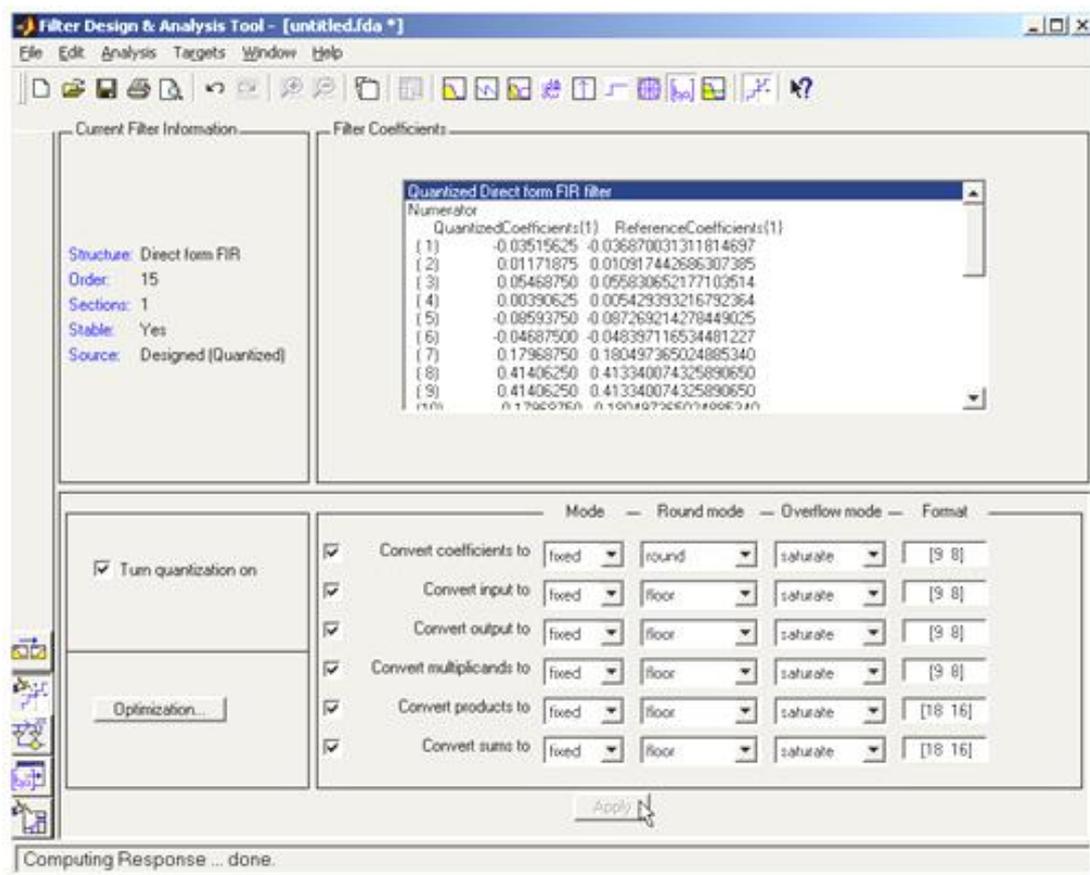


图 12-16 量化参数设置

12.1 FIR数字滤波器设计

12.1.3 使用MATLAB的滤波器设计工具

4. 量化



图 12-17 量化优化设置

12.1 FIR数字滤波器设计

12.1.3 使用MATLAB的滤波器设计工具

4. 量化

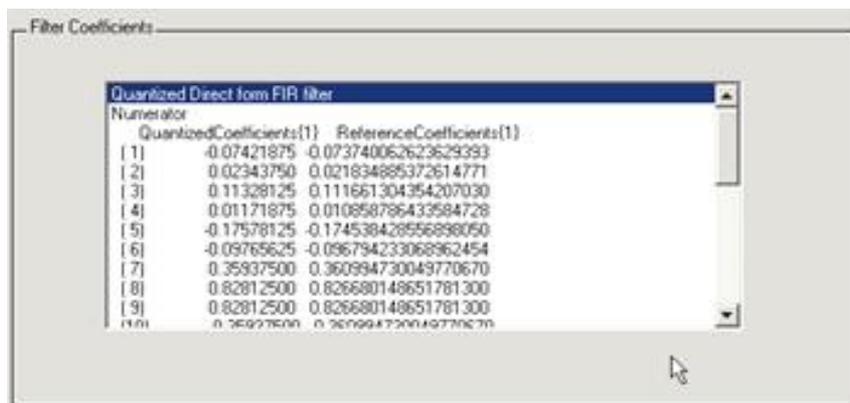


图 12-18 量化后系数

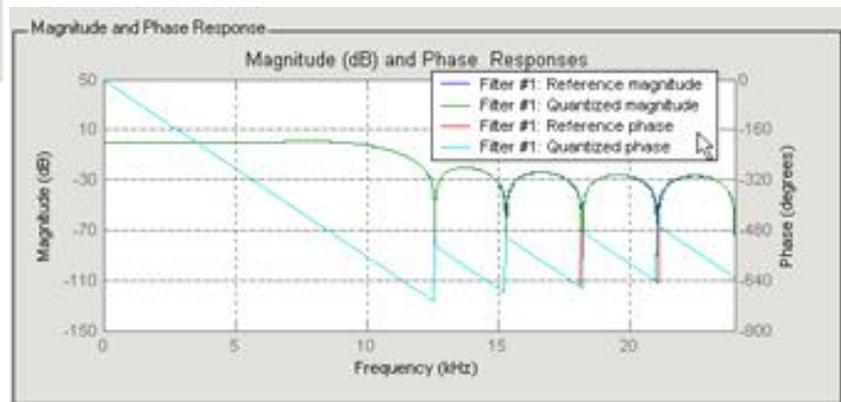


图 12-19 量化后幅频、相频响应

12.1 FIR数字滤波器设计

12.1.3 使用MATLAB的滤波器设计工具

4. 量化

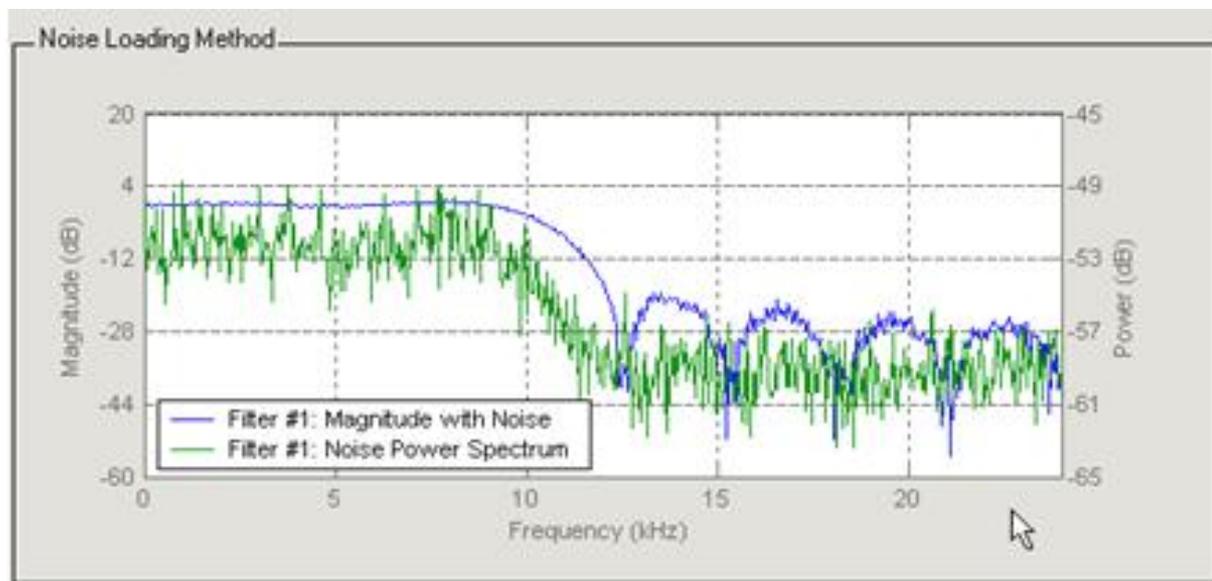


图 12-20 量化后噪声分析

12.1 FIR数字滤波器设计

12.1.3 使用MATLAB的滤波器设计工具

5. 导出滤波器系数

```
Num =  
-0.0742    0.0234    0.1133    0.0117   -0.1758   -0.0977  
 0.3594    0.8281    0.8281    0.3594   -0.0977   -0.1758  
 0.0117    0.1133    0.0234   -0.0742
```

```
>> Num*(2^8)  
ans =  
Columns 1 through 10  
-19     6    29     3   -45   -25    92   212   212    92  
Columns 11 through 16  
-25   -45     3    29     6   -19
```



图 12-21 导出对话框

12.1 FIR数字滤波器设计

12.1.3 使用MATLAB的滤波器设计工具

6. 修改FIR滤波器模型添加参数

7. 导出滤波器系数的另一种方法

12.1 FIR数字滤波器设计

12.1.4 使用FIR IP Core设计FIR滤波器

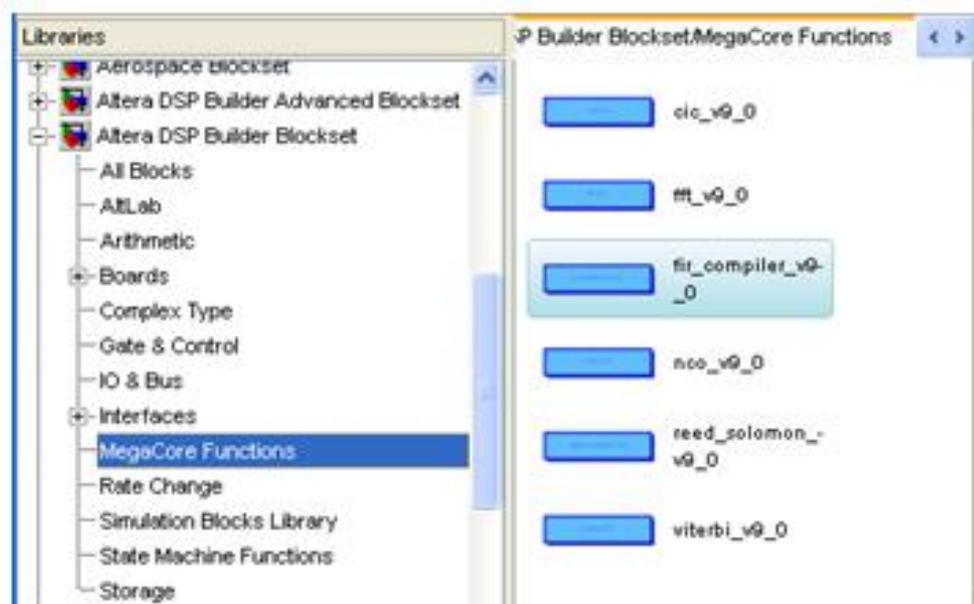


图 12-22 IP Core 模块库

12.1 FIR数字滤波器设计

12.1.4 使用FIR IP Core设计FIR滤波器

1. FIR滤波器核的使用
2. 配置FIR滤波器器核



图 12-23 设置 FIR Core 参数

12.1 FIR数字滤波器设计

The screenshot shows the 'Parameterize - FIR Compiler' dialog box. The main window is titled 'Coefficients Specification - (Low Pass Set [1])'. It features a central plot area showing the frequency response of the filter. The plot has two curves: a blue line for 'Floating Coeff. Response' and a green line for 'Fixed Coeff. Response'. The y-axis is labeled '0dB' at the top and '-120' at the bottom. The x-axis is labeled 'Frequency' and ranges from 0 to 0.5. The plot shows a low-pass filter response with a passband ripple and a stopband attenuation. Below the plot, there are tabs for 'Frequency Response' (selected) and 'Time Response & Coefficient Values'. To the right of the plot, there are several configuration sections: 'Rate Specification' (Single Rate, Factor 2), 'Input Specification' (Number of Input Channels: 1, Input Number System: Signed Binary, Input Bit Width: 8), and 'Output Specification' (Full Resolution Bit Width is 21, Based on Method: Actual Coefficients, Output Number System: Full Resolution). At the bottom, there is an 'Architecture Specification' section with dropdowns for Device Family (Cyclone III), Structure (Distributed Arithmetic: Fully Parallel Filter), Pipeline Level (1), Data Storage (Logic Cells), and Coefficient Storage (Auto). A resource utilization table is also visible, showing 780 Logic Cells and 0 Multipliers. The dialog box has 'Cancel' and 'Finish' buttons at the bottom right.

Figure 12-24 shows the 'Parameterize - FIR Compiler' dialog box, which is used to configure the FIR filter design. The dialog is divided into several sections:

- Coefficients Specification - (Low Pass Set [1])**: Includes buttons for 'New Coefficient Set', 'Edit Coefficient Set', and 'Remove Coefficient Set'. It shows a plot of the filter's frequency response, comparing 'Floating Coeff. Response' (blue line) and 'Fixed Coeff. Response' (green line). The plot shows the magnitude response in dB versus Frequency (0 to 0.5). Below the plot are tabs for 'Frequency Response' (selected) and 'Time Response & Coefficient Values'. The 'Coefficients Scaling' is set to 'Auto' and the 'Bit Width' is 10.
- Rate Specification**: Includes 'Single Rate' and 'Factor 2'.
- Input Specification**: Includes 'Number of Input Channels' (1), 'Input Number System' (Signed Binary), and 'Input Bit Width' (8).
- Output Specification**: Includes 'Full Resolution Bit Width is 21', 'Based on Method' (Actual Coefficients), and 'Output Number System' (Full Resolution).
- Architecture Specification**: Includes 'Device Family' (Cyclone III), 'Structure' (Distributed Arithmetic: Fully Parallel Filter), 'Pipeline Level' (1), 'Data Storage' (Logic Cells), and 'Coefficient Storage' (Auto). It also includes a resource utilization table and a throughput section.

Resource	Utilizatio...
Logic Cells	780
M512	0
M4K	0
M-RAM	0
M9K	0
M144K	0
MLAB	0
Multipliers	0

Throughput (Fully Streaming):

- An input data is processed every 1 clock periods.
- A new output data is generated every clock period.

图 12-24 确定 FIR 滤波器系数

12.1 FIR数字滤波器设计

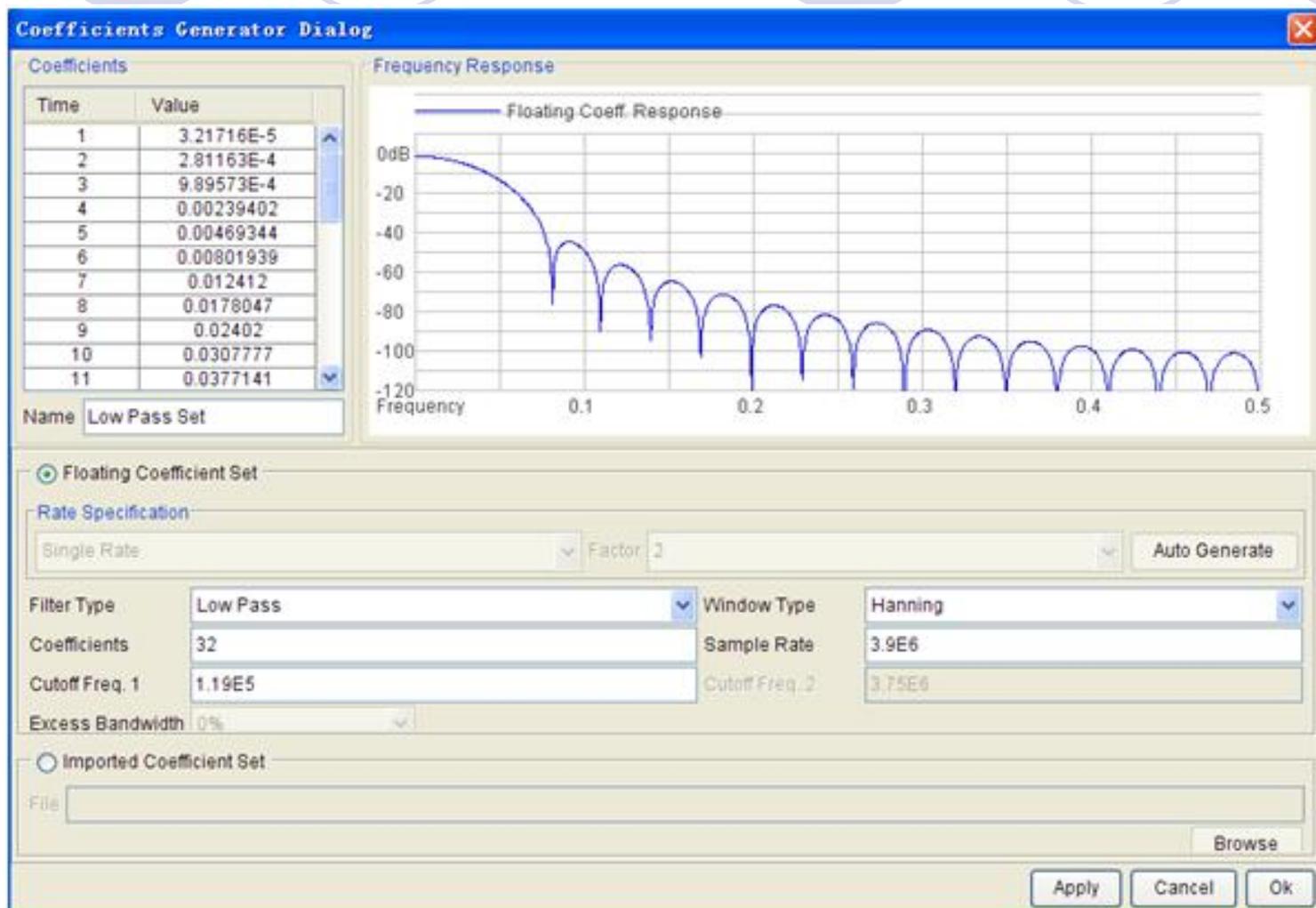


图 12-25 确定 FIR 工作方式

12.1 FIR数字滤波器设计

12.1.4 使用FIR IP Core设计FIR滤波器

2. 配置FIR滤波器器核

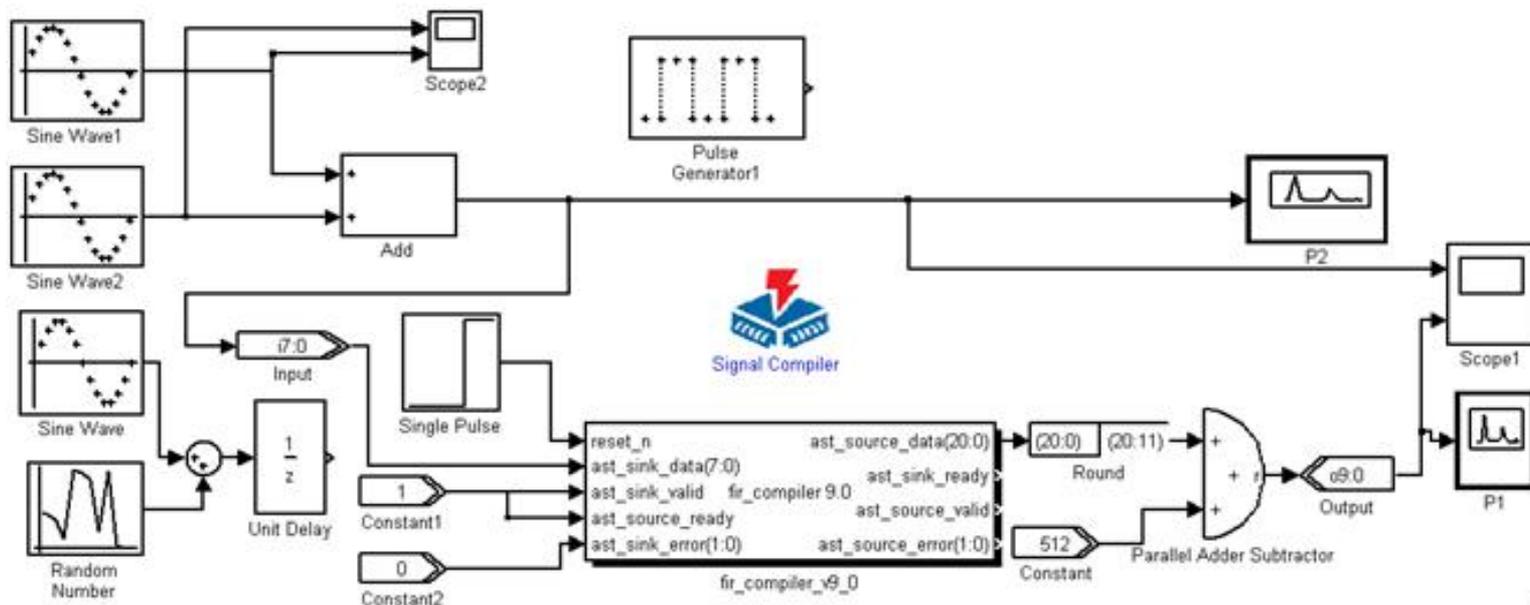


图 12-26 FIR 滤波器核的测试电路模型

12.1 FIR数字滤波器设计

12.1.4 使用FIR IP Core设计FIR滤波器

2. 配置FIR滤波器器核

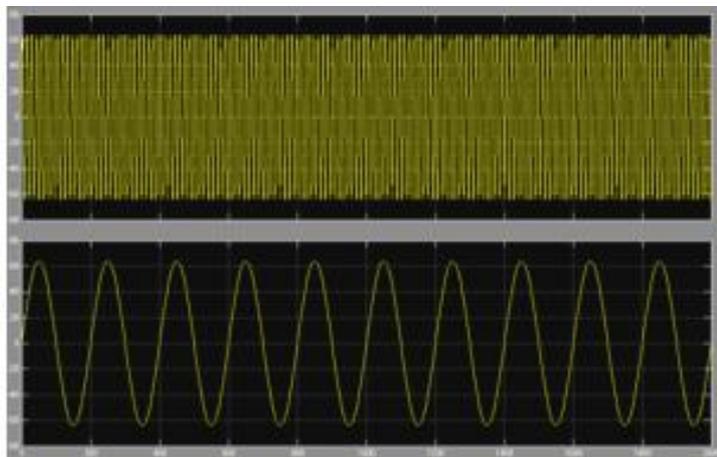


图 12-27 Scope2 显示波形

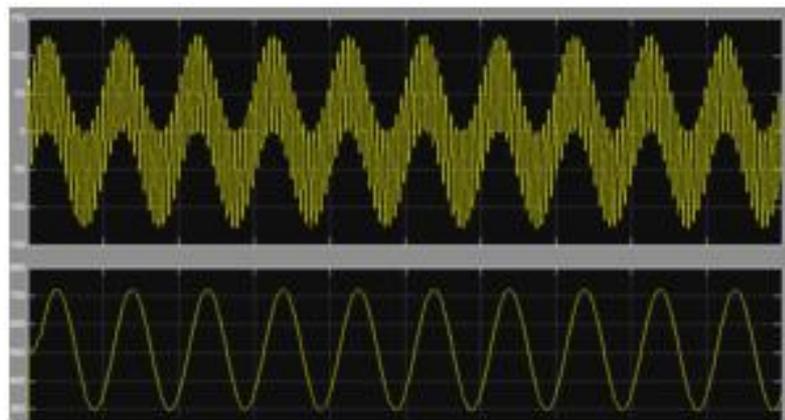


图 12-28 Scope1 显示波形

12.1 FIR数字滤波器设计

12.1.4 使用FIR IP Core设计FIR滤波器

2. 配置FIR滤波器器核

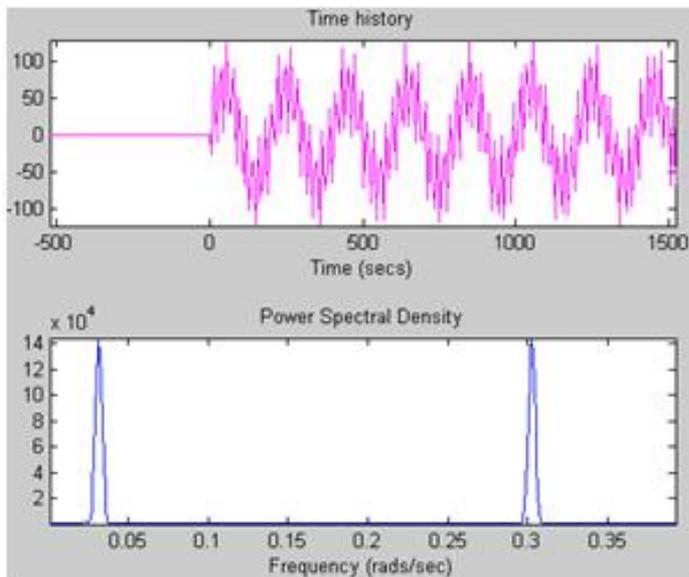


图 12-29 P2 频谱仪显示波形

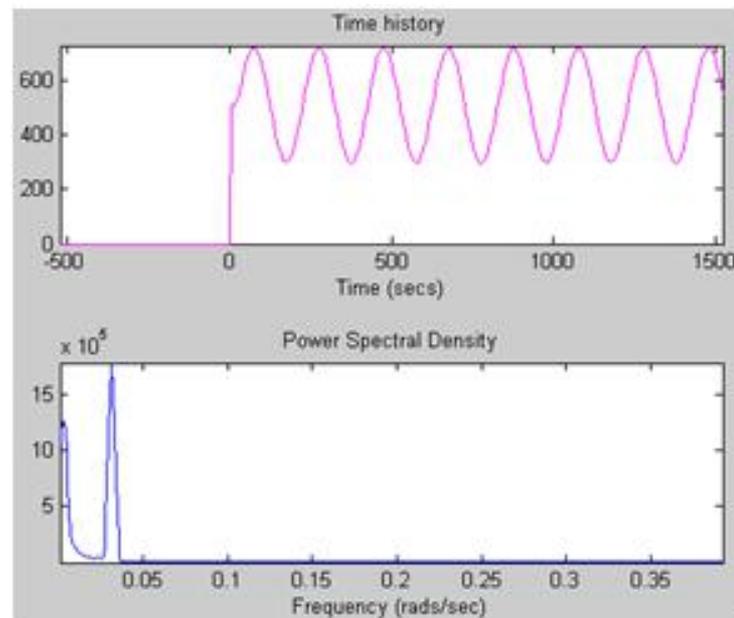


图 12-30 P1 频谱仪显示波形

12.2 HDL模块插入仿真及其设计

1. 完成Verilog HDL设计

【例 12-1】

```
module MUX21a (A,B,S,Y);  
    input S ; input [7:0]A,B;    output [7:0]Y;  
    reg [7:0] Y;+  
    always @(A,B,S) begin  
        if (S==0) Y = A; else Y = B;+  
    end  
endmodule
```

12.2 HDL模块插入仿真及其设计

2. 调入HDL Import模块

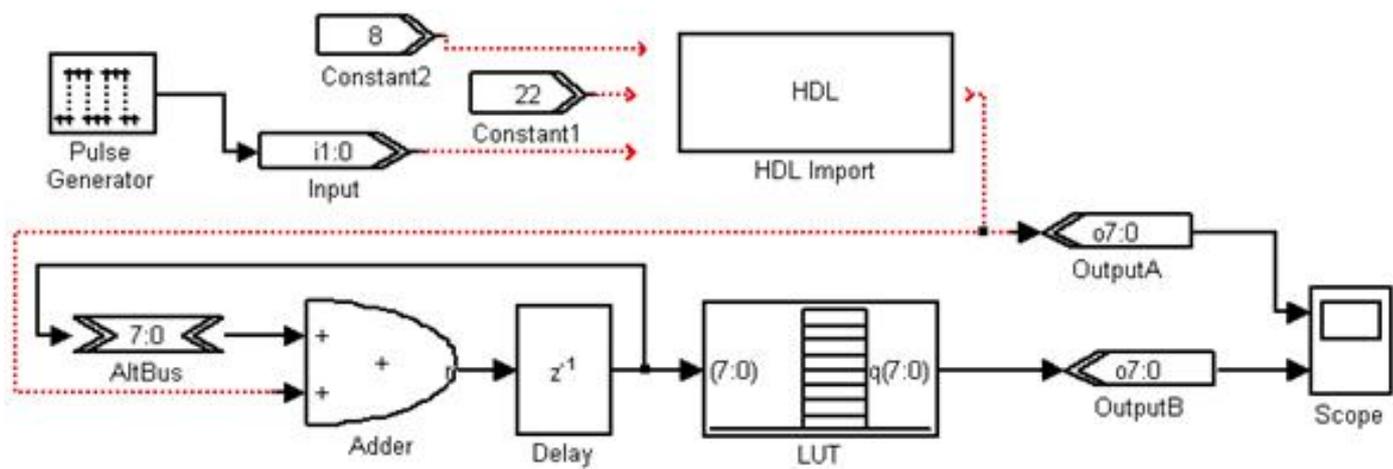


图 12-31 在 FSK 的 Simulink 模型中调入一个 HDL Import 模块

12.2 HDL模块插入仿真及其设计

3. 加入Verilog设计文件



图 12-32 加入 Verilog 文件



图 12-33 选中设计好的文件

12.2 HDL模块插入仿真及其设计

4. 仿真

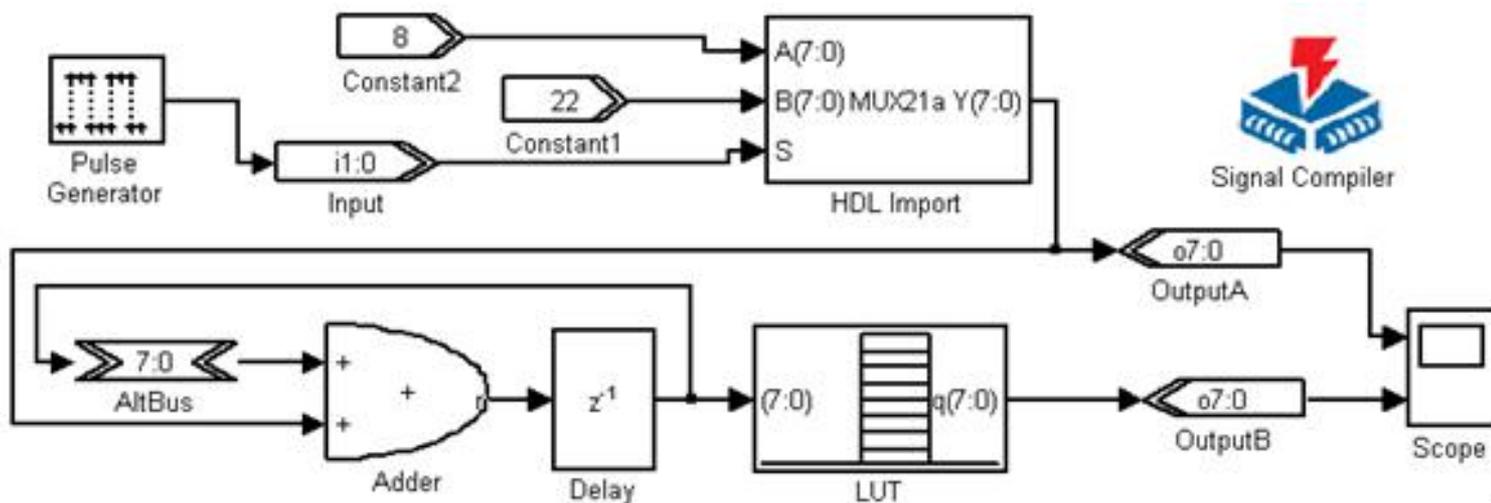


图 12-34 构成一个完整设计

习题

$$x[i] = \sum_{k=0}^{31} X[k] * \cos \left[\frac{i+16}{64} \pi(2k+1) \right], i=0 \cdots 63$$

$$x[i] = \sum_{k=0}^{31} X[k] * \cos \left[\frac{i * \pi}{64} \pi(2k+1) \right], i=0 \cdots 31$$

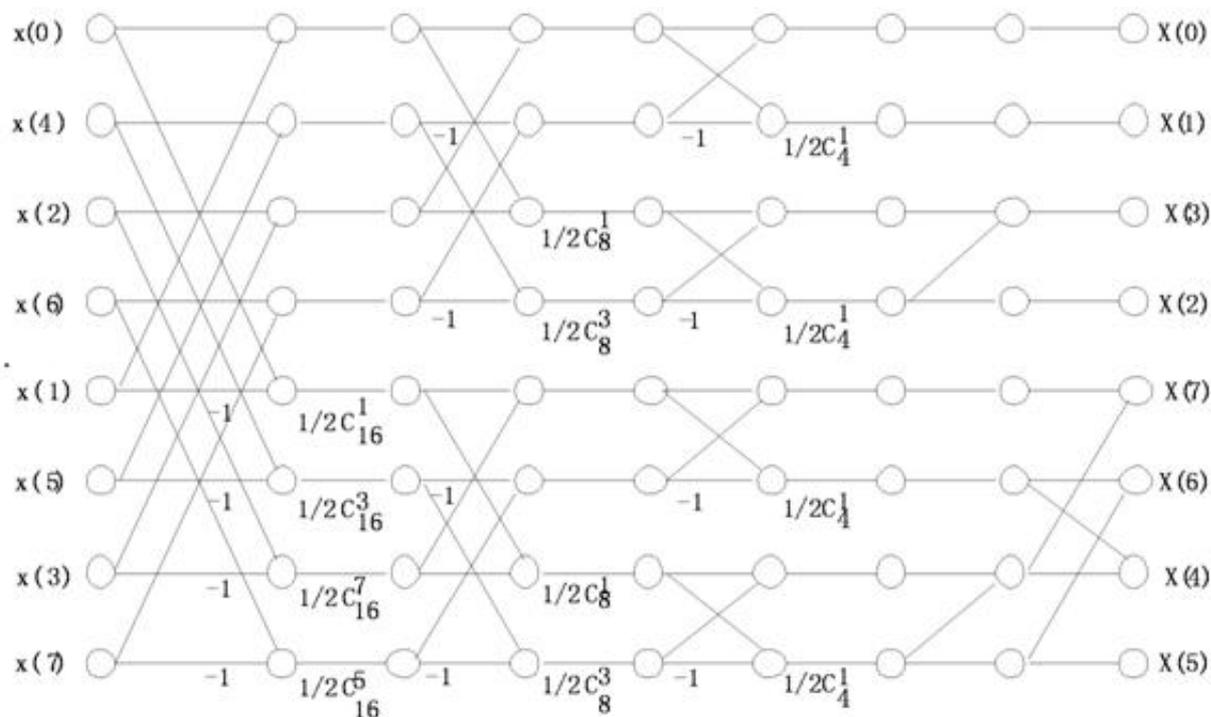


图 12-35 Lee 氏快速 DCT 算法

实验与设计

实验12-1 FIR数字滤波器设计实验

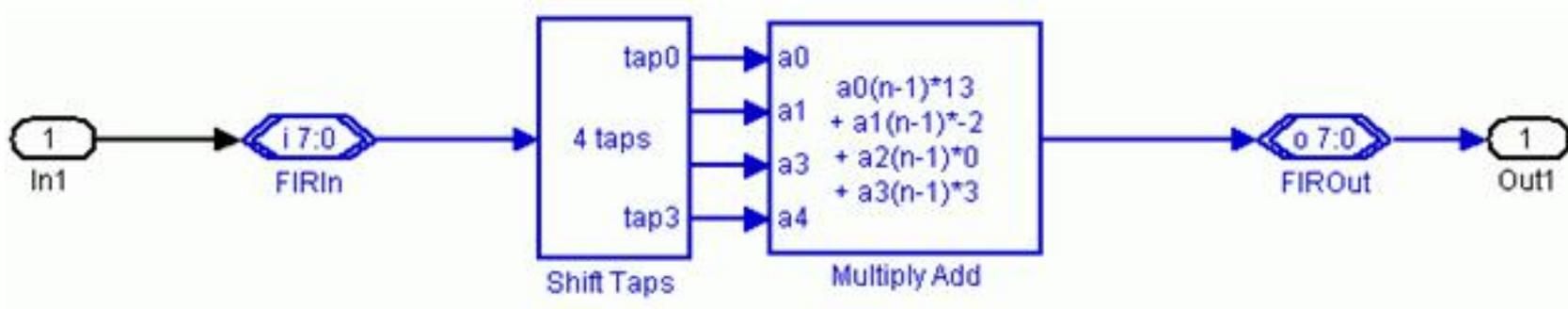


图 12-36 Shift Taps 模块和 Multiply Add 模块应用

实验12-2 HDL Import模块应用实验